

Industriefunkuhren



Technical Manual
OEM Sync-Module FE1000
(IRIG-B)

ENGLISH

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Version Number (Firmware / Manual)

THE FIRST TWO DIGITS OF THE VERSION NUMBER OF THE TECHNICAL MANUAL AND THE FIRST TWO DIGITS OF THE FIRMWARE VERSION MUST **COMPLY WITH EACH OTHER.**

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Symbols and Characters



Operational Reliability

Disregard may cause damages to persons or material.



Functionality

Disregard may impact function of system/device.



Information

Notes and Information.



Safety regulations

The safety regulations and observance of the technical data serve to ensure trouble-free operation of the device and protection of persons and material. It is therefore of utmost importance to observe and compliance with these regulations.

If these are not complied with, then no claims may be made under the terms of the warranty. No liability will be assumed for any ensuing damage.



Safety of the device

This device has been manufactured in accordance with the latest technological standards and approved safety regulations

The device should only be put into operation by trained and qualified staff. Care must be taken that all cable connections are laid and fixed in position correctly. The device should only be operated with the voltage supply indicated on the identification label.

The device should only be operated by qualified staff or employees who have received specific instruction.

If a device must be opened for repair, this should only be carried out by employees with appropriate qualifications or by **hopf** Elektronik GmbH.

Before a device is opened or a fuse is changed all power supplies must be disconnected.

If there are reasons to believe that the operational safety can no longer be guaranteed the device must be taken out of service and labelled accordingly.

The safety may be impaired when the device does not operate properly or if it is obviously damaged.

CE Conformity



This device fulfils the requirements of the EU directive 89/336/EEG "Electromagnetic compatibility" and 73/23/EEG "Low voltage equipment".

Therefore the device bears the CE identification marking (CE=Communauté Européenne)

CE = Communautés Européennes = European communities

The CE indicates to the controlling bodies that the product complies with the requirements of the EU directive - especially with regard to protection of health and safety for the operator and the user - and may be released for sale within the common markets.

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1 General

The IRIG-B Module FE1000 is a compact IRIG-B converter for the integration into Clock Systems and signal converters. This module converts the time information of an externally fed IRIG-B signal (analogue/digital) into a serial string based on the **hopf** Master/Slave string.

Furthermore, internally synchronized pulses, as PPS (pulse per second) and 1kHz frequency are put out.

The module can be synchronized via different IRIG Time Code formats:

- IRIG-B according to IRIG Standard 200-98 (this format does not include any year date)
- IRIG-B according to IRIG Standard 200-04
- IEEE 1344-1995
- AFNOR NF S87-500

It is possible to connect both analogue and digital IRIG-B signals to the Module.



In order to guarantee a successful synchronization, IRIG-B Module FE1000 requires for approx. 2-3 minutes an undisturbed signal. As the module has no internal back-up clock and in order to receive an internal time, it is required to synchronize the module after a reset or a power failure again.

The according status of the module is shown by two LEDs in the front panel enabling to identify a successful or rather a disturbed synchronisation visually.

The internal signal output of the time information of Module FE1000 depends on the appropriate synchronization status and also on internal settings.

2 Informational Content of the IRIG-B / IEEE1344 / AFNOR Formats

Following items should be considered referring to time synchronization via an IRIG-B signal:

1. The different IRIG-B formats, as IEEE1344 and AFNOR NF S87-500 provide beside the time different information that are transferred.
2. Not all formats support the transmission of the year date which are important for a complete indication of time and date.



The IRIG-B Module FE1000 can be parameterised so that the module either uses the year date provided by the fed IRIG-B signal or by the appropriate Clock System.

2.1 IRIG-B Formats without Year Date

The "old" IRIB-B formats according to Standard 200-98 **do not** contain any information on the current year.

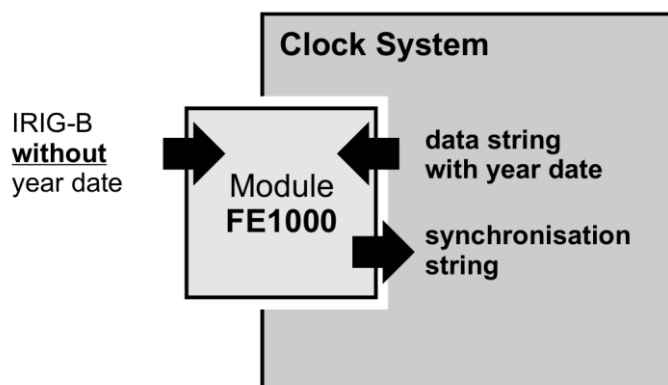
These formats are Bxx0, Bxx1, Bxx2 and Bxx3.



Using these formats the module must be adjusted to "year date provided by the Clock System".

A wrong adjustment results in the use of a **wrong year** in the System.

2.1.1 Functional Principle of Module FE1000 for IRIG-B without Year Date



2.2 IRIG-B / IEEE1344 / AFNOR Formats with Year Date

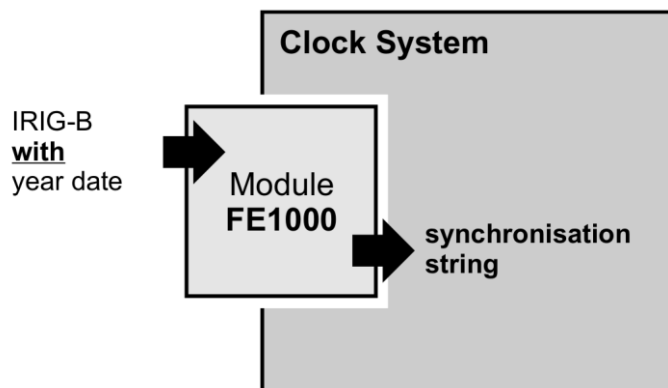
The current IRIG Standard 200-04 has been extended by 4 formats providing the year date.

These formats are Bxx4, Bxx5, Bxx6 and Bxx7.

These formats include the implementation of additional information instead of the control function.

The formats IEEE1344 and AFNOR NF S87-500 also include the year date necessary for synchronization.

2.2.1 Functional Principle of Module FE1000 for IRIG-B with Year Date



3 Design of Module FE1000

3.1 Front Panel Elements of Module FE1000



Status Optical Coupler

3 pole pluggable screw terminal
Plug connector

Pin	Signal TTL (Jumper J1= 1-2)	Signal RS422 (Jumper J1= 2-3)
1	TTL - Input	RxD+ (high-active)
2	Must remain free!	RxD- (low-active)
3	GND potential free	GND potential free

Status LEDs

LED	Meaning
RD	Status LED red
GN	Status LED green

IRIG-B Analogue

BNC connector female

IRIG-B	Analogue signal input
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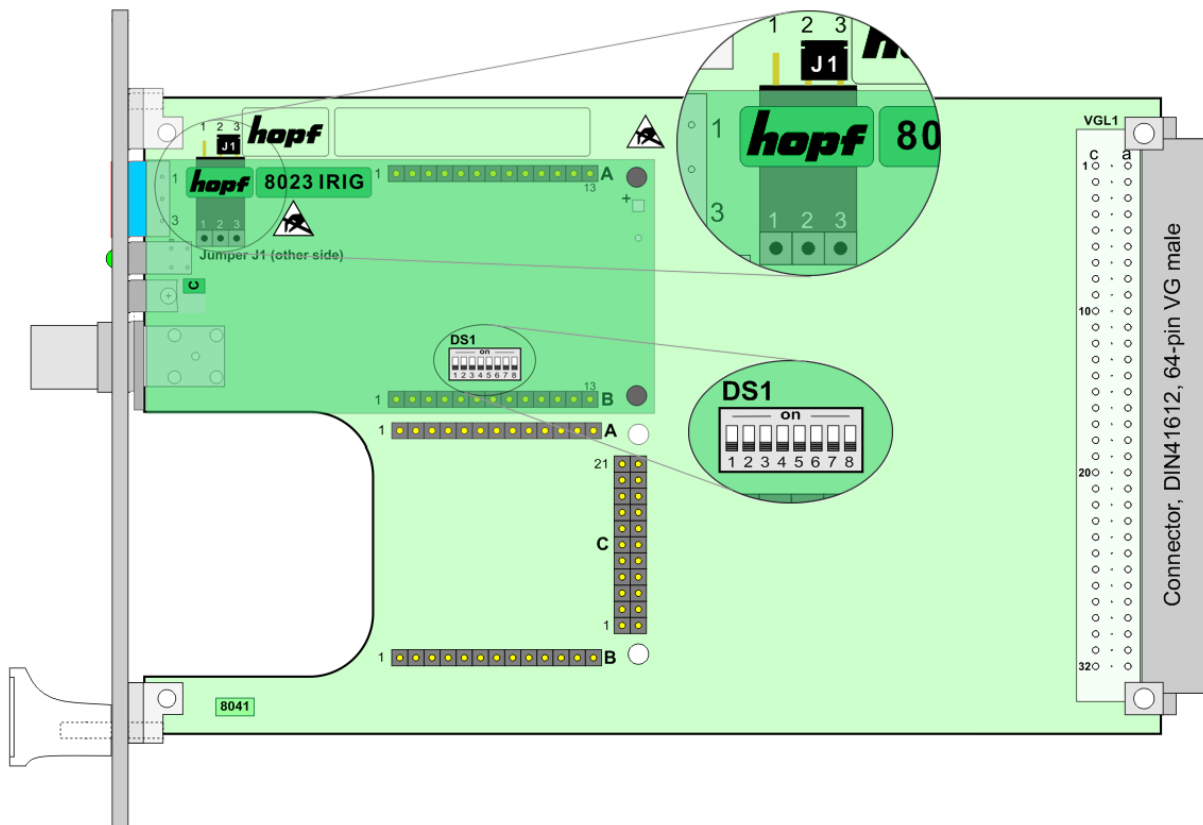


Configuration of jumper J1 for input signals at TTL level requires as a matter of necessity and for a faultless operation that Pin 2 of the connecting plug must remain free.



The selection whether the digital or the analogue input signal for synchronisation is used is made via an internal DIP switch DS1.

3.2 Overview of Module FE1000



3.2.1 Jumper J1 – Input level for IRIG-B Digital Signal

Via jumper J1 the selection of the digital IRIG-B signal is made.

- 1 – 2 Input signal at TTL level
- 2 – 3 Input signal at RS422 level



Configuration of jumper J1 for input signals at TTL level requires as a matter of necessity and for a faultless operation that Pin 2 of the connecting plug "RIG-B Digital" must remain free.

3.2.2 DIP Switch DS1

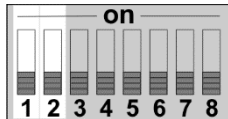
Several settings are made by means of DIP switch DS1.

3.2.2.1 DIP Switch 1+2 / Selection of Data String for Year Date

The Module FE1000 can receive the year date from different serial data strings.



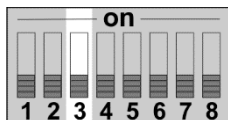
Only effective with DS1 SW3 = ON



SW1	SW2	Function
ON	ON	hopf Master/Slave String – every second
ON	OFF	BUS-String System 7001RC
OFF	ON	hopf Master/Slave String – every minute
OFF	OFF	BUS-String System 6000/7001

3.2.2.2 DIP Switch 3 / Year Date from IRIG-B or Clock System

Adjustment in which way the Module FE1000 receives the year date.



SW3	Function
ON	Year date used from the respective Clock System
OFF	Year date used out of IRIG-B signal

3.2.2.3 DIP Switch 4 / Year Date used from Memory

This function determines the reaction of the module adjusted to "year date from the Clock System" when the data string transmitted to the module does not include the required year date (for example the Clock System itself does not provide a valid time/date information).



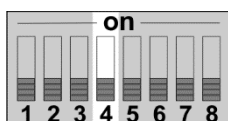
Only effective with DS1 SW3 = ON

With the function "year date only used out of data string" active, synchronous status of the module is not given until the year date is received via the adjusted serial data string.

With the function "year date used from memory" active, the module waits 5 minutes after switching on or reset on the adjusted data string with the year date. When the data string is not received after 5 minutes or does not include the required information, the module uses the last valid year date from the internal fail-safe memory.



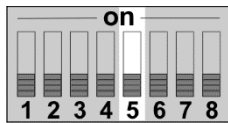
With the function "year date only used out of data string" active, for synchronization the user's intervention is mandatorily required in case e.g. the Clock System has no valid information on the back-up clock after a turn off of several days.



SW4	Function
ON	Year date only used out of data string
OFF	Year date used from memory

3.2.2.4 DIP Switch 5 / Evaluation of digital or analogue IRIG-B Signal

Adjustment whether the IRIG-B signal input for the synchronization of the Module FE1000 is made via the analogue or digital input.

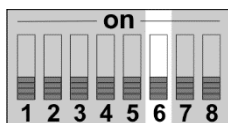


SW5	Function
ON	The analogue IRIG-B signal is evaluated
OFF	The digital IRIG-B signal is evaluated

3.2.2.5 DIP Switch 6 / Currently No Function



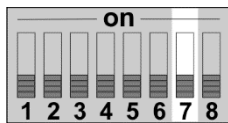
For compatibility reasons the switch should always be set to OFF



SW6	Function
ON	Currently no function
OFF	Currently no function (Default)

3.2.2.6 DIP Switch 7 / String Output Only in Status Sync

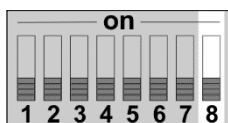
Adjustment whether the output of internal synchronization string should be steadily (independent of the synchronization status and availability of a valid time information) or only in status **Sync.** of Module FE1000.



SW7	Function
ON	Independent of the status a string is always transmitted
OFF	Only in status sync. A string is transmitted (Default)

3.2.2.7 DIP Switch 8 / String Output every second or every minute

The transmission cycle of the output **hopf** Master/Slave String can be set to every second or every minute depending on the demands of the Clock System to be synchronized.



SW8	Function
ON	String output every second
OFF	String output every minute (Default)

4 Commissioning

This chapter is about commissioning of the IRIG-B Module FE1000.



Usually the IRIG-B Module FE1000 is parameterized by default that only the required settings for the input IRIG-B signal needed to be executed.

4.1 Step 1: IRIG-B Input Signal ANALOGUE / DIGITAL

Via the DIP-Switch DS1 the setting is made whether the IRIG-B is processed for synchronization via the analogue or digital input.

4.2 Step 2: Year Date used from the Clock System or the IRIG-B Signal

Via the DIP-Switch DS1 the setting must be made whether the available IRIG-B signal necessary for the synchronization provides the required year date.

4.2.1 Extended Settings for Mode: Year provided by the Clock System

With the function "year date out of Clock System" active a differentiated behaviour of the Module FE1000 for the various applications can be set.

This adjustment defines whether after switching on or a RESET a valid time is available in the Clock System (for example the Clock System has no back-up clock or was off for more than 3 days).

Adjustment "Year date only used out of Data String"

Using this setting the Module FE1000 only becomes synchronous and thus the Clock System if the module receives a valid year date via the data string of the Clock System.



If there is no valid time or date available in the Clock System the user must set a valid time for synchronisation.

Adjustment "Year dated used from Memory"

In this adjustment the Module FE1000 uses the last valid year date from the internal fail-safe memory for synchronisation in case the module **does not** receive a valid year date via the data string of the Clock System after a time period of 5 minutes after turning on or a RESET.



If a wrong year should be displayed in the system using these settings the following procedure should be executed:

- Disconnect the IRIG-B cable from the FE1000 module
- Enter the needed time and date via the clock system and let the system run over the next minute change
- The FE1000 module needs a reset in order to take over the new time and date. Therefore the clock system has to be switched off for 5 seconds and then switched on again.
- Afterwards the IRIG-B cable can be re-connected to the FE1000 module

4.3 Step 3: Behaviour of the Output String of Module FE1000

The behaviour of the internal output of the synchronization (**hopf** Master/Slave String) can be set via DIP switch DS1.

4.3.1 Transmission Cycle EVERY SECOND/ EVERY MINUTE

The transmission cycle of the output **hopf** Master/Slave String can be set to every second or every minute depending on the demands of the Clock Systems to be synchronized.

4.3.2 Transmission ALWAYS / ONLY IN STATUS SYNC

This adjustment determines whether the connected Clock System is synchronized as soon as there is a valid time information available in Module FE1000 or only while the Module FE1000 is synchronized via the IRIG-B signal.

5 Status LEDs

For a better failure analysis the Status LEDs show a different behaviour in the two general operation modes (year date from Clock System / year date out of IRIG-B signal).

5.1 Status LEDs – Mode: Year Date from Clock System

The Status LEDs on the front panel indicate the current (synchronization) status of the board. The LEDs have the following meaning:

LED Red	LED Green	Status
OFF	ON	Sync (radio synchronous) with crystal control
ON	1Hz	Year available + no input signal
2Hz	1Hz	Year available + signal not evaluable / not yet evaluated
5Hz	1Hz	No year available + input signal OK
ON	OFF	No year available + no input signal

5.2 Status LEDs – Mode: Year Date out of IRIG-B Signal

The Status LEDs on the front panel indicate the current (synchronization) status of the board. The LEDs have the following meaning:

LED Red	LED Green	Status
OFF	ON	Sync (radio synchronous) with crystal control
5Hz	OFF	no input signal
2Hz	OFF	signal not evaluable / not yet evaluated

6 Evaluable IRIG-B / IEEE1344 / AFNOR Input Signals

The following telegrams / Time Code formats can be evaluated by Module FE1000:

- IRIG-B according to IRIG Standard 200-98
- IRIG-B according to IRIG Standard 200-04
- IEEE 1344-1995
- AFNOR NF S87-500

Analogue Signals (for example IRIG-B 12x):

- Modulation depth 3:1
- Voltage level 1 - 10 V_{pp}

Digital Signals (for example IRIG-B 00x):

optionally

- RS422 level

or

- TTL level

6.1 IRIG-B according to IRIG Standard 200-98

The IRIG-B format consists of a time code of 74 bits and a repeat rate of one second. The bit frame is 10msec. The quality rating of a bit is marked by the pulse width modulation and is a multiple of a millisecond.

For synchronisation on the beginning of the second a neutral logical condition is required named identifier.

- | | |
|--------------|-----------------|
| • Logical 0 | = 2msec H-level |
| • Logical 1 | = 5msec H-level |
| • Identifier | = 8msec H-level |

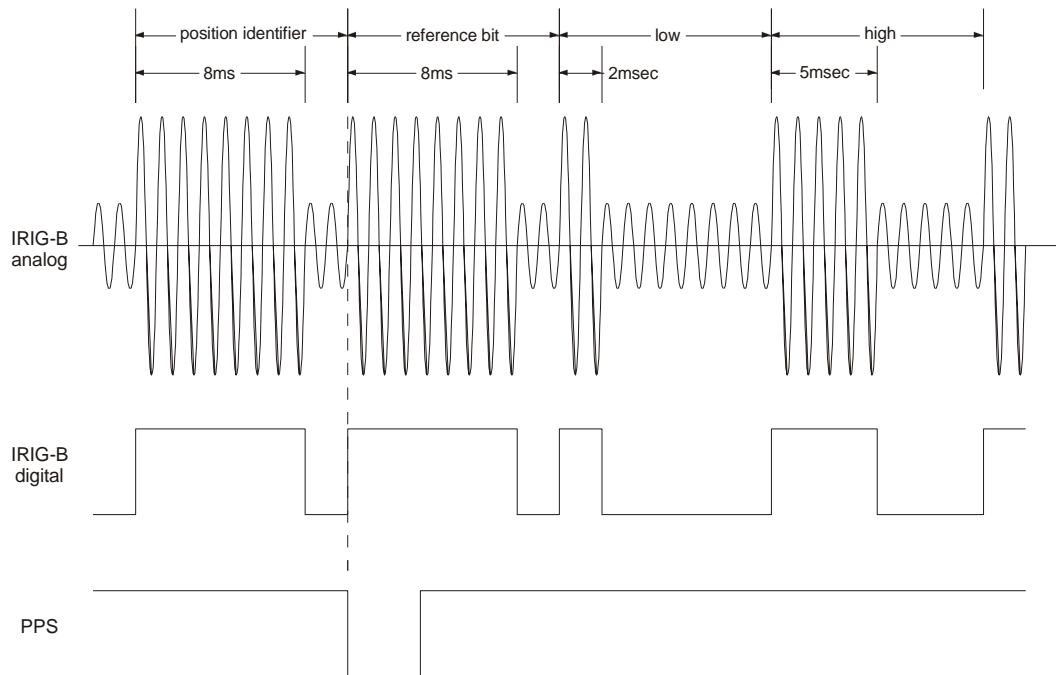
The 74 time code bits are divided into

- 30 bits for the BCD value of the seconds, minutes and hours and the current day of the year
- 27 bits for the input of control information
- 17 bits for the binary value of the current seconds of the day

Within one second 100 bit frames can be transferred. Not used bit frames are completed with a logical zero.

Information referring to the year, difference time UTC to local time and status daylight saving time / winter time are not included in the telegram according to IRIG Standard 200-98.

The below drawing shows the IRIG-B signal quality rating in analogue and digital format.



6.2 IRIG-B according to IRIG Standard 200-04

The IRIG-B Standard 200-04 is an extension of the Standard 200-98. Additional IRIG telegrams with extended information were defined.

For example, the current year is additionally sent in the first control information field. That enables the issue of a complete time/date information.

6.3 IEEE 1344-1995

This version of the IRIG Standard is an extension of the IRIG Standard 200-98. The 27 bits of the control information field are occupied with fixed data as year, time offset between UTC and local time, daylight saving time / winter time status etc. It is downward compatible to Standard 200-98 (the IRIG Standard 200-98 is included as a subset).

6.4 AFNOR NF S87-500

This IRIG standard is issued by the French Institute of Engineering Standard and is built up on the Standard IRIG 200-98 auf. 27 bits of the control information field are occupied with fixed data as year, month etc. It is downward compatible to Standard 200-98 (the IRIG Standard 200-98 is included as a subset).

7 Technical Data

General Data	
Operating voltage:	5V DC \pm 5%
Temperature: Storage / Operating	-20 ... +85°C / 0 ... +70°C
Humidity:	95%, not condensed
Standards:	CE
Protection class:	none
MTBF:	> 900,000 hours
Conversion accuracy:	
Analogue-Signal:	\pm 20 μ sec, Jitter \pm 5 μ sec
Digital-Signal:	\pm 3 μ sec
Freewheel Stability:	\pm 0.2ppm to input signal after 0.5 hours of continuous IRIG-B signal reception

Signal Inputs	
IRIG-B analogue:	Potential separation 500V DC
Impedance:	10kOhm
Voltage level:	1 - 10V _{pp}
Degree of modulation:	3 : 1
IRIG-B digital:	Potential separation 500V DC
Voltage level:	RS422, TTL-level Automatic recognition of high- and low-active signals
IRIG Format:	- IRIG-B according to IRIG Standard 200-98 - IRIG-B according to IRIG Standard 200-04 - IEEE1344-1955 - AFNOR NFS 87-500 With automatic format recognition
Internal Serial Interface:	TTL-level

Signal Outputs:	
PPS-Pulse:	TTL-level high-active
Pulse width:	50msec
1kHz-Signal:	TTL-level 50/50 low-active
Serial interface:	TTL-level low-active